Amendment(s) to the Claims

Please amend the claims to read as follows. *Note that all claim numbers are indicated consistent with the Examiner's renumbering in the prior action.*

29. (Original) A context switch controller in a processor that includes an operand data storage for holding data operated upon by instructions executing on the processor, the operand data storage being divided into a plurality of storage groups containing one or more storage elements, the context switch controller comprising:

a dirty bit storage including one or more storage bits that correspond to one or more respective storage groups in the operand data storage; and

a dirty bit logic coupled to the dirty bit storage and coupled to receive a destination address field of the instructions, the dirty bit logic responsive to an executed instruction by classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction and by evaluating the classified destination based on whether the instruction updates the targeted storage group.

30. (Original) A context switch controller according to Claim 29 wherein:

the dirty bit logic is responsive to a context switch by saving storage groups based on the evaluation of the classified destinations.

31. (Cancelled).

32. (Cancelled).

33. (Currently Amended) A context switching logic in a processor that includes operand data ~~an executive~~ storage for holding operand data operated upon by instructions executing on the processor, the operand data ~~executive~~ storage being divided into a plurality of storage groups containing one or more storage elements, the context switching logic comprising:

means for utilizing a dirty bit storage including a plurality of storage bits corresponding to a plurality of respective storage groups in the operand data ~~executive~~ storage;

means for receiving a destination address field of the executing instructions;

means for responsive to an executed instruction, classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction; and

means for evaluating the classified destination based on whether the instruction updates the targeted storage group. ~~; and~~

~~means responsive to a context switch for saving storage groups based on the evaluation of the classified destinations.~~

34. (Currently Amended) A context switch controller in a processor, the context switch controller comprising:

a data storage unit divided into a plurality of storage groups;

a dirty bit storage coupled to the data storage and including one or more storage bits corresponding to ~~one or more~~ respective ones of storage groups in the data storage unit, wherein operation of the context switch controller is based, at least in part, on state of the dirty bit storage; and

a dirty bit logic coupled to the dirty bit storage and configured to receive a destination address of one or more instructions executing on the processor.

35. (Original) The context switch controller of claim 34 wherein the dirty bit logic is responsive to one or more instructions executed on the processor to

classify a destination access as a targeted storage group according to information in a destination address field of the one or more instructions executed on the processor; and

evaluate the classified destination address based on whether the instruction updates the targeted storage group.

36. (Original) The context switch controller of claim 35, wherein

the dirty bit logic is responsive to a context switch by saving the storage groups based on the evaluation of the classified destinations.

37. (Original) The context switch controller of claim 34, wherein the data storage unit is configured to hold data operated by the one or more instructions executed on the processor.

38. (Original) The context switch controller of claim 34, wherein each one of the plurality of storage groups comprises one or more storage elements.